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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/572,799	03/22/2006	Dimitri Lederer	LEDE3001/JEK	4919

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EXAMINER	
SLUTSKER, JULIA	

ART UNIT	PAPER NUMBER
4193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/572,799	LEDERER ET AL.	
	Examiner	Art Unit	
	JULIA SLUTSKER	4193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/22/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 31 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 31, the wording "remains...after standard CMOS process" is unclear, since it does not point out what a standard CMOS process is. Additionally, the claim fails to point out the method's steps which ensure the claimed behavior of the material such as "density of charge trap remains higher than or equal to $10^{11}/cm^2/eV$.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 20-24, 27-33 and 35-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA).

Regarding claims 20, Auberton-Herve teaches a method of manufacturing of a multilayer semiconductor structure and a multilayer semiconductor structure comprising a silicon substrate (Fig.5c, numeral 3), an active semiconductor layer (Fig.5c, numeral 10) and an insulating layer

(Fig.5c, numeral 16) in between the silicon substrate and the active semiconductor layer, wherein the method comprises suppressing ohmic losses inside silicon substrate by increasing charge trap density between the insulating layer and the silicon substrate (page 3, [0044]).

Auberton-Herve does not teach that the silicon substrate has a resistivity higher than 3KΩ.cm. However, AAPA discloses the use high-resistivity substrates with resistivity higher than 3KΩ.cm (Spec., page 2, lines 15-22). Thus, it would have been obviose to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve reference by combining with AAPA to have the silicon substrate with a resistivity higher than 3KΩ.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding claim 32, Auberton-Herve teaches a multilayer structure comprising a silicon substrate (Fig.5c, numeral 3), an active semiconductor layer (Fig.5c, numeral 10) and an insulating layer (Fig.5c, numeral 16) in between the silicon substrate and the active semiconductor layer, wherein the multilayer structure comprises an intermediate layer (Fig.5a, numerals, 5, 6) in between the high resistivity silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088])) preferably smaller than 50 nm.

Auberton-Herve does not teach that the silicon substrate has a resistivity higher than 3KΩ.cm. However, AAPA discloses the use high-resistivity substrates with resistivity higher than 3KΩ.cm (Spec., page 2, lines 15-22). Thus, it would have been obviose to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve reference by combining

with AAPA to have the silicon substrate with a resistivity higher than 3KΩ.cm for the purpose of reducing losses and coupling in high-frequency applications (Spec., page 2, lines 16-22).

Regarding claim 21, in the combination above Auberton-Herve teaches increasing charge trap density comprises applying an intermediate layer (Fig.5a, numerals, 5, 6)in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, preferably smaller than 50 nm (implicit in page 5, [0084], [0085], note: thickness of the polycrystalline layer in Fig.1, 50 nm (page 5, [0088])).

Regarding claims 22 and 33, the combination Auberton-Herver and AAPA does not teaches that the intermediate layer has a charge trap density of at least 10^{11}/cm2/eV, preferably at least 10^{12}/cm2/eV. However, it would have been obvious to one of ordinary skill in the art at time the invention was made to adjust the charge trap density to at least 10^{11}/cm2/eV for the purpose of increasing efficiency of the gettering layer.

Regarding claims 23 and 35, in the combination above, Auberton-Herver that applying an intermediate layer comprises applying any of an undoped or lightly doped silicon layer, an undoped polysilicon layer in between the silicon substrate and the insulating layer (page 5, [0084], [0085]).

Regarding claims 24 and 36, in the combination above, Auberton-Herver teaches that the intermediate layer having an RMS roughness, wherein the RMS roughness of the intermediate layer has an average value smaller than or equal to 0.5 nm (it has been disclosed that the intermediate layer (Fig.5, numerals 5,6 consist of a polycrystalline material (numeral 5) covered

with amorphous silicon (numeral 6) to obtain a surface with very low roughness (page 6, [0115], page 7, [0123], [0127]).

Regarding claims 27, in the combination above, Auberton-Herver teaches bonding (Fig.5 a to b) an intermediate layer-covered high resistivity silicon substrate (Fig.5, numeral 3) to an insulator-passivated semiconductor substrate (Fig.5, numeral 12).

Regarding claim 28, in the combination above Auberton-Herver teaches oxidation of a surface of the intermediate layer prior to bonding the high resistivity silicon substrate to the insulator-passivated semiconductor substrate (page 5, [0074], polishing).

Regarding claim 29, in the combination above, Auberton-Herver teaches providing an intermediate layer (Fig.5, numeral 5,6) on an insulator-passivated semiconductor substrate (Fig.5, numeral 3), and bonding this to a high-resistivity silicon substrate (Fig.5, numeral 12).

Regarding claim 30, in the combination above, Auberton –Herver teaches that the intermediate layer has a layer thickness of at least 100 nm (page 5, [0092]).

Regarding claim 31, the combination of AAPA and Auberton-Herver does not teach that the density of charge traps remains higher than or equal to $10^{11}/cm^2/eV$ after a standard CMOS process is performed on the structure. However it would have been obvious to one of ordinary skill in the art at time the invention was made to have density of charge traps remains higher than or equal to $10^{11}/cm^2/eV$ after a standard CMOS process is performed on the structure for the purpose of preserving integrity of CMOS.

Regarding claim 37, in the combination above, Auberton- Herver teaches that the active semiconductor layer is made from at least of Si (page 6, [0109]).

Regarding claim 38, in the combination above, Auberton-Herver teaches that the insulating layer is formed of at least one of an oxide (page 6, [0112]).

5. Claims 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA) as applied to claim 24 above, and further in view of Inoue et al. (EP 104452 A1, hereinafter "Inoue").

Regarding claim 25, Auberton-Herve in view of AAPA teaches all limitations of claim 24 for reasons above. Auberton-Herve in view of AAPA does not teaches that applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer. Inoue teaches that applying a polysilicon layer comprises depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer (column 13, [0085], [0087]). Thus, it would have been obvious to one of ordinary skill in the art at time the invention was made to modify Auberton-Herve in view of AAPA and to apply a polysilicon layer by depositing amorphous silicon on the silicon substrate and crystallizing the amorphous silicon so as to form the polysilicon layer s taught by Inoue for the purpose of decreasing of damage during ion implantation (Inoue, column 20[0088]).

Regarding claim 26, in the combination above, Inoue teaches that crystallizing comprises any of thermal annealing or rapid thermal annealing (RTA) or laser crystallization (column 19, [0085]).

6. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Auberton-Herve (US 2003/0129780) in view of Applicant Admission of the Prior Art (AAPA) as applied to claim 32 above, and further in view of Shiota et al (EP 0975011 A, hereinafter "Shiota").

Regarding claim 34, the combination of Auberton-Herve and AAPA does not teaches that the multilayer structure has an effective resistivity higher than 5KΩCm. However, Shiota teaches that the multilayer structure has an effective resistivity higher than 5KΩCm (column 13, [0108], column 17, [0143]). Thus, it would have been obvious to one of ordinary skill in the art at time the invention was made to modify combination of Auberton-Herve and AAPA to have the multilayer structure has an effective resistivity higher than 5KΩCm as taught by Shiota for the purpose reducing losses and coupling in high-frequency applications (AAPA, Spec., page 2, lines 16-22).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Usenko (US Patent 6,368,938)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Taghi Arani can be reached on 571-272-3787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

/Taghi T. Arani/
Supervisory Patent Examiner, Art Unit 4193
4/30/2008